Amendments to the Claims

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Canceled)

2. (Currently amended) A semiconductor device, comprising:

a semiconductor chip provided with an integrated circuit and a pad that is electrically connected to the integrated circuit;

a wiring layer that has ~~a~~ an etched concave portion and is electrically connected to the pad;

an external terminal that is joined to the concave portion of the wiring layer; and

a resin layer provided with a through hole and disposed on the wiring layer, the through hole and the concave portion residing at the same position,

wherein a width of the concave portion increases with a depth of the concave portion.

3. (Currently amended) A semiconductor device, comprising:

a semiconductor chip provided with an integrated circuit and a pad that is electrically connected to the integrated circuit;

a wiring layer that has ~~a~~ an etched concave portion and is electrically connected to the pad;

an external terminal that is joined to the concave portion of the wiring layer; and

a resin layer provided with a through hole and disposed on the wiring layer, the through hole and the concave portion residing at the same position,

wherein the concave portion has a first width at a first depth and a second width at a second depth that is deeper than the first depth, the first width being larger than an opening size of the concave portion and the second width being smaller than the first width.

4. (Previously presented) The semiconductor device according to claim 2, wherein an inner surface of the through hole in the resin layer is in contact with the external terminal.

5. (Previously presented) The semiconductor device according to claim 2, further comprising a stress relaxation layer disposed on the semiconductor chip, wherein the wiring layer is disposed on the stress relaxation layer.

6. (Previously presented) The semiconductor device according to claim 2, wherein the resin layer is prepared from a solder resist.

7. (Previously presented) A circuit board comprising a semiconductor device according to claim 2.

8. (Previously presented) An electronic apparatus comprising a semiconductor device according to claim 2.

9. (Canceled)

10. (Currently amended) A semiconductor wafer, comprising:

a semiconductor substrate provided with a plurality of integrated circuits and pads with each pad electrically connected to each of the integrated circuits;

a wiring layer that has a an etched concave portion and is electrically connected to the pads;

an external terminal that is joined to the concave portion of the wiring layer; and

a resin layer provided with a through hole and disposed on the wiring layer, the through hole and the concave portion residing at a same position,

wherein a width of the concave portion increases with a depth of the concave portion.

11. (Currently amended) A semiconductor wafer, comprising:

a semiconductor substrate provided with a plurality of integrated circuits and pads with each pad electrically connected to each of the integrated circuits;

a wiring layer that has a an etched concave portion and is electrically connected to the pads;

an external terminal that is joined to the concave portion of the wiring layer; and

a resin layer provided with a through hole and disposed on the wiring layer, the through hole and the concave portion residing at a same position,

wherein the concave portion has a first width at a first depth and a second width at a second depth that is deeper than the first depth, the first width being larger than an opening size of the concave portion and the second width being smaller than the first width.

12. (Previously presented) The semiconductor wafer according to claim 11, wherein an inner surface of the through hole in the resin layer is in contact with the external terminal.

13. (Previously presented) The semiconductor wafer according to claim 11, further comprising a stress relaxation layer disposed on the semiconductor substrate, wherein the wiring layer is disposed on the stress relaxation layer.

14. (Previously presented) The semiconductor wafer according to claim 11, wherein the resin layer is prepared from a solder resist.

15-20. (Canceled)